Document number: MC34710
Rev 4, 8/2008

RoHS

# Dual Output DC-DC & Linear Regulator IC

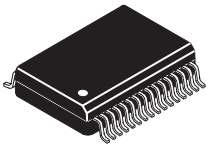
**34710**

**DUAL OUTPUT DC-DC & LINEAR REGULATOR**

The 34710 is a dual-output power regulator IC integrating switching regulator, linear regulator, supervisory and power supply sequencing circuitry. With a wide operating input voltage range of 13 to 32V, the 34710 is applicable to many commercial and industrial applications using embedded MCUs.

A mode-selected 5.0or 3.3V DC-DC switching regulator is provided for board-level I/O and user circuitry up to 700mA. A linear regulator provides mode-selected core supply voltages of either 3.3V, 2.5V,1.8V, or 1.5V at currents up to 500mA.

The supervisor circuitry ensures that the regulator outputs follow a predetermined power-up and power-down sequence.



**EW SUFFIX (PB-FREE)**
**98ASA10627D**
**32-PIN SOICW**

### Features

- Efficient 5.0V/3.3V buck regulator
- Low Noise LDO Regulator (mode-selected 3.3V, 2.5V,1.8V, or 1.5V)
- On-chip thermal shutdown circuitry
- Supervisory functions (Power-ON Reset and Error Reset circuitry)
- Sequenced I/O and core voltages
- Pb-free packaging designated by suffix code EW

| ORDERING INFORMATION | | |
|---|---|---|
| **Device** | **Temperature Range ($T_A$)** | **Package** |
| MC34710EW/R2 | 0°C to 85°C | 32 SOICW-EP |

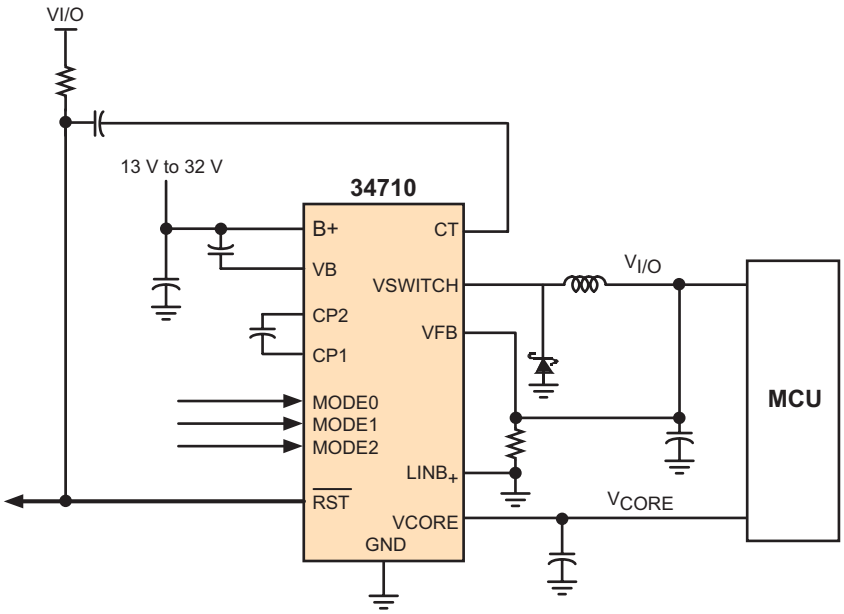



**Figure 1. 34710 Simplified Application Diagram**

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.



freescale semiconductor

# INTERNAL BLOCK DIAGRAM

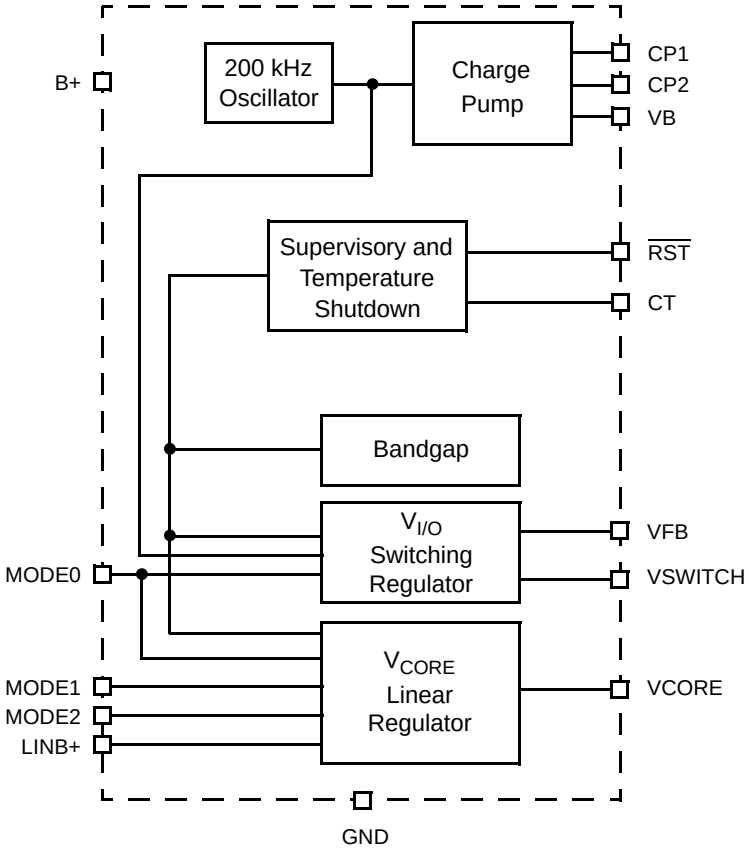



**Figure 2. 34710 Simplified Internal Block Diagram**

# PIN CONNECTIONS

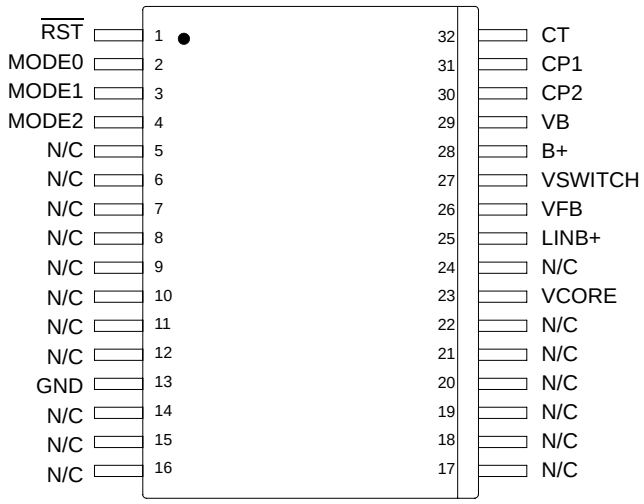



**Figure 3. 34710 Pin Connections**

**Table 1. 34710 Pin Definitions**

| Pin Number | Pin Name | Pin Function | Formal Name | Definition |
|---|---|---|---|---|
| 1 | $\overline{\text{RST}}$ | Reset | Reset | Reset is an open drain output only. |
| 2<br>3<br>4 | Mode0<br>Mode1<br>Mode2 | Input | Mode Control | These input pins control $V_{FB}$ and $V_{CORE}$ output voltages. |
| 5–12,<br>14–22, 24 | NC | NC | No Connects | No internal connection to this pin. |
| 13 | GND | Ground | Ground | Ground. |
| 23 | VCORE | Output | Core Voltage Regulator Output | Core regulator output voltage. |
| 25 | LINB+ | Input | Core Voltage Regulator Input | Core regulator input voltage. |
| 26 | VFB | Input | $V_{I/O}$ Switching Regulator Feedback | Feedback pin for $V_{I/O}$ switching regulator and internal logic supply. |
| 27 | VSWITCH | Output | $V_{I/O}$ Switching Regulator Switch Output | $V_{I/O}$ switching regulator switching output. |
| 28 | B+ | Input | Power Supply Input | Regulator input voltage. |
| 29 | VB | Output | Boost Voltage | Boost voltage storage node. |
| 30 | CP2 | Passive Component | CP Capacitor Positive | Charge pump capacitor connection 2. |
| 31 | CP1 | Passive Component | CP Capacitor Negative | Charge pump capacitor connection 1. |
| 32 | CT | Passive Component | Reset Delay Capacitor | Reset delay adjustment capacitor. |

# ELECTRICAL CHARACTERISTICS

## *MAXIMUM RATINGS*

**Table 2. MAXIMUM RATINGS**

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

| Rating | Symbol | Max | Unit |
|---|---|---|---|
| **ELECTRICAL RATINGS** | | | |
| Input Power Supply Voltage<br>$I_{B+}$ = 0.0A | $V_{B+}$ | -0.3 to 36 | V |
| Peak Package Reflow Temperature During Reflow(1), (2) | $T_{PPRT}$ | Note 2 | °C |
| Power Dissipation(3) | $P_D$ | 3.0 | W |
| ESD Standoff Voltage<br>Non-Operating, Unbiased, Human Body Model(4) | $V_{ESD1}$ | ±2000 | V |
| Thermal Resistance<br>Junction-to-Ambient(5)<br>Junction-to-Ambient(3)<br>Junction-to-Exposed-Pad | <br>$R_{\theta JA}$<br>$R_{\theta JA}$<br>$R_{\theta JC}$ | <br>45<br>25<br>2.0 | °C/W |
| **THERMAL RATINGS** | | | |
| Operating Ambient Temperature | $T_A$ | 0 to 85 | °C |
| Operating Junction Temperature | $T_J$ | 0 to 105 | °C |
| Input Power Supply Voltage<br>$I_{B+}$ = 0.0A to 3.0A | $V_{B+}$ | 13 to 32 | V |
| Quiescent Bias Current from B+(6)<br>$V_{B+}$ = 13 to 32V | $I_{B+}(Q)$ | 7.5 | mA |
| **$V_{I/O}$ SWITCHING REGULATOR(7)** | | | |
| Maximum Output Voltage Startup Overshoot ($C_{OUT}$ = 330µF)<br>Mode0 = 0<br>Mode0 = Open | $V_{I/O}(STARTUP)$ | <br>5.4<br>3.6 | V |
| Maximum Output Current<br>$T_A$ = 0°C to 105°C | $I_{VI/O}$ | 700 | mA |

Notes

1. ESD testing is performed in accordance with the Human Body Model (HBM) ($C_{ZAP}$ = 100 pF, $R_{ZAP}$ = 1500 Ω), the Machine Model (MM) ($C_{ZAP}$ = 200 pF, $R_{ZAP}$ = 0 Ω), and the Charge Device Model (CDM), Robotic ($C_{ZAP}$ = 4.0pF).
2. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
3. With 2.0 $in^2$ of copper heatsink.
4. ESD1 testing is performed in accordance with the Human Body Model ($C_{ZAP}$ = 100pF, $R_{ZAP}$ = 1500Ω).
5. With no additional heatsinking.
6. Maximum quiescent power dissipation is 0.25W.
7. 13V ≤ $V_{B+}$ ≤ 32V and -20°C ≤ $T_J$ ≤ 145°C, unless otherwise noted.

**Table 2. MAXIMUM RATINGS (continued)**

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

| Rating | Symbol | Max | Unit |
|---|---|---|---|
| **$V_{CORE}$ LINEAR REGULATOR**[8] | | | |
| Maximum Output Voltage Startup Overshoot ($C_{OUT}$ = 10μF) [9]<br>Mode2=Low, Mode1=Low, Mode0=Low<br>Mode2=Open, Mode1=Low, Mode0=Don't Care<br>Mode2=Low, Mode1=Open, Mode0=Don't Care<br>Mode2=Open, Mode1=Open, Mode0=Don't Care | $V_{CORE}$(STARTUP) | <br>3.6<br>2.7<br>2.0<br>1.65 | V |
| Maximum Output Current<br>$T_J$ = 0°C to 105°C, $V_{LINB+} \leq V_{CORE}$(NOM) + 0.8V[10] | $I_{VCORE}$ | <br>500 | mA |

Notes

8. 13V ≤ $V_{B+}$ ≤ 32V and -20°C ≤ $T_J$ ≤ 145°C, unless otherwise noted.
9. Refer to Table 5, page 9.
10. Pulse testing with low duty cycle used.

## *STATIC ELECTRICAL CHARACTERISTICS*

**Table 3. STATIC ELECTRICAL CHARACTERISTICS**

Characteristics noted under conditions 4.75V ≤ $V_{IO}$ ≤ 5.25V, 13V ≤ $V_{B+}$ ≤ 32V, and 0°C ≤ $T_J$ ≤ 105°C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A$ = 25°C under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **SWITCHING REGULATOR (VI/O, MODE0)** | | | | | |
| Logic Supply Voltage ($I_{VI/O}$ = 25 to 700mA) | $V_{I/O}$ | | | | V |
| Mode0 = 0 | | 4.8 | 5.0 | 5.2 | |
| Mode0 = Open (floating) | | 3.15 | 3.25 | 3.45 | |
| Output On Resistance | $R_{DS(ON)}$ | | | | Ω |
| $V_{B+}$ = 13 to 32V | | 0.5 | 1.0 | 2.0 | |
| Soft Start Threshold Voltage | $V_{I/O}$(SOFT) | | | | V |
| Mode0 = any | | – | 2.5 | 3.1 | |
| Current Limit Threshold ($T_J$ = 25°C to 100°C) | | | | | A |
| Normal Operation | $I_{LIMIT}$(OP) | 1.9 | 2.4 | 2.9 | |
| Soft Start, $V_{I/O}$ ≤ 2.5V | $I_{LIMIT}$(SOFT) | 1.0 | – | 1.9 | |
| Minimum Voltage Allowable on $V_{SWITCH}$ Pin | $V_{VSWITCH}$(MIN) | | | | V |
| $T_J$ = 25°C to 100°C | | -0.5 | – | – | |
| **LINEAR REGULATOR (VCORE, MODE 1, 2, 3, 4)** | | | | | |
| Supply Voltage ($I_{VCORE}$ = 5.0mA)[11] | $V_{CORE}$(NOM) | | | | V |
| Mode2=Low, Mode1=Don't Care, Mode0=Low | | 3.15 | 3.3 | 3.45 | |
| Mode2=Low, Mode1=Don't Care, Mode0=Open | | 2.45 | 2.5 | 2.75 | |
| Mode2=Open, Mode1=Don't Care, Mode0=Low | | 1.7 | 1.8 | 2.05 | |
| Mode2=Open, Mode1=Don't Care, Mode0=Open | | 1.425 | 1.5 | 1.575 | |
| Supply Voltage ($I_{VCORE}$ = 500mA)[11] | $V_{CORE}$(NOM) | | | | V |
| Mode2=Low, Mode1=Don't Care, Mode0=Low | | 3.0 | – | 3.4 | |
| Mode2=Low, Mode1=Don't Care, Mode0=Open | | 2.2 | – | 2.6 | |
| Mode2=Open, Mode1=Don't Care, Mode0=Low | | 1.55 | – | 1.9 | |
| Mode2=Open, Mode1=Don't Care, Mode0=Open | | 1.33 | – | 1.53 | |
| $V_{CORE}$ Dropout Voltage | $I_{VCORE}$(DROPOUT) | | | | V |
| $V_{CORE}$ = $V_{CORE}$(NOM), $I_{VCORE}$ = 0.5A | | – | 0.5 | 0.8 | |
| Normal Current Limit Threshold | $I_{LIMIT}$ | | | | mA |
| $T_J$ = 25°C to 100°C, $V_{LINB+}$ = $V_{CORE}$(NOM) + 1.0V | | 600 | 800 | 1000 | |

Notes

11. Refer to Table 5, page 9.

**Table 3. STATIC ELECTRICAL CHARACTERISTICS (continued)**

Characteristics noted under conditions 4.75V ≤ $V_{IO}$ ≤ 5.25V, 13V ≤ $V_{B+}$ ≤ 32V, and 0°C ≤ $T_J$ ≤ 105°C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A$ = 25°C under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **MODE PINS OPERATING VOLTAGES** | | | | | |
| Mode Control Pins Low Voltage | $V_{IL}(Mode_n)$ | – | – | 0.825 | V |
| Mode Control Pins High Voltage | $V_{IH}(Mode_n)$ | 2.6 | – | – | V |
| Mode Control Pins Voltage with Input Floating<br>$V_{B+}$ = 13 to 14V | $V_{Mode}$(FLOAT) | 7.0 | 8.0 | 13 | V |
| **SUPERVISOR CIRCUITRY ($\overline{RST}$, VCORE)** | | | | | |
| Minimum Function $V_{B+}$ for Charge Pump and Oscillator Running | $V_{B+}$(MIN) | – | – | 9.0 | V |
| Minimum $V_{B+}$ for $\overline{RST}$ Assertion, $V_{B+}$ Rising | $V_{B+}$(ASSERT) | – | 1.9 | 2.2 | V |
| $\overline{RST}$ Low Voltage<br>$V_{B+}$ = 2.0V, $I_{\overline{RST}}$ ≤ 5.0mA | $V_{OL}$ | – | 0.25 | 0.4 | V |
| $\overline{RST}$ $V_{I/O}$ Threshold<br>$V_{I/O}$ Rising<br>$V_{I/O}$ Falling | <br>$V_{I/OT+}$<br>$V_{I/OT-}$ | <br>–<br>$V_{I/O}$(NOM) - 300mV | <br>–<br>– | <br>$V_{I/O}$(NOM) - 50mV<br>– | V |
| $\overline{RST}$ Hysteresis for $V_{I/O}$ | $V_{HYSVI/O}$ | 10 | – | 100 | mV |
| $\overline{RST}$ $V_{CORE}$ Threshold<br>$V_{CORE}$ Rising<br>$V_{CORE}$ Falling | <br>$V_{CORET+}$<br>$V_{CORET-}$ | <br>–<br>$V_{CORE}$(NOM) - 300mV | <br>–<br>– | <br>$V_{CORE}$(NOM) - 30mV<br>– | V |
| $\overline{RST}$ Hysteresis for $V_{CORE}$<br>$V_{B+}$ = 13 to 32V | $V_{HYS\ CORE}$ | 10 | 50 | 100 | mV |
| $V_{CORE}$ - $V_{I/O}$ for $V_{CORE}$ Shutdown<br>$V_{B+}$ = 13 to 32V | $V_{CORE}$(SHUTDOWN) | 0.5 | – | 0.9 | V |
| Thermal Shutdown Temperature<br>$T_J$ Rising | $T_J$(TSD) | – | – | 170 | °C |
| Over-temperature Hysteresis | $T_J$(HYSTERESIS) | – | 20 | – | °C |
| **VB CHARGE PUMP** | | | | | |
| Boost Voltage[12]<br>$V_{B+}$ = 12 V, $I_{vb}$ = 0.5 mA<br>$V_{B+}$ = 32 V, $I_{vb}$ = 0.5 mA | <br>$V_B$<br>$V_B$ | <br>$V_{B+}$ 8<br>$V_{B+}$ 10 | <br>$V_{B+}$ 9<br>$V_{B+}$ 12 | <br>$V_{B+}$ 10<br>$V_{B+}$ 14 | V |

Notes

12. Bulk capacitor ESR ≤ 10 milliohms

## *DYNAMIC ELECTRICAL CHARACTERISTICS*

**Table 4. DYNAMIC ELECTRICAL CHARACTERISTICS**

Characteristics noted under conditions 4.75V ≤ $V_{IO}$ ≤ 5.25V, 13V ≤ $V_{B+}$ ≤ 32V, and 0°C ≤ $T_J$ ≤ 105°C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A$ = 25°C under nominal conditions unless otherwise noted

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **$V_{I/O}$ SWITCHING REGULATOR** | | | | | |
| Duty Cycle | D | 45 | 49 | 55 | % |
| Switching Rise and Fall Time<br>Load Resistance = 100Ω, $V_{B+}$ = 30V | $t_R$, $t_F$ | <br>20 | <br>35 | <br>50 | ns |
| **SUPERVISOR CIRCUITRY (RST)** | | | | | |
| $\overline{RST}$ Delay<br>$C_{delay}$ = 0.1μF | $t_{DELAY}$ | <br>40 | <br>60 | <br>80 | ms |
| $\overline{RST}$ Filter Time<br>$V_{B+}$ = 9.0V | $t_{FILTER}$ | <br>2.0 | <br>4.0 | <br>8.0 | μs |
| $\overline{RST}$ Fall Time<br>$C_L$ = 100pF, $R_{PULLUP}$ = 4.7kΩ, 90% to 10% | $t_F$ | <br>– | <br>25 | <br>75 | ns |
| C Delay<br>Charge Current<br>Threshold Voltage | <br>$I_{CDLY}$<br>$V_{THCD}$ | <br>2.0<br>1.7 | <br>3.5<br>2.0 | <br>5.0<br>2.2 | <br>μA<br>V |
| **INTERNAL OSCILLATOR** | | | | | |
| Charge Pump and $V_{I/O}$ Switching Regulator Operating Frequency<br>$V_{B+}$ = 12 to 32V | $f_{OP}$ | <br>140 | <br>170 | <br>260 | kHz |

# FUNCTIONAL DESCRIPTION

## *INTRODUCTION*

### $V_{I/O}$ Switching Regulator

The $V_{I/O}$ switching regulator output voltage is determined by the Mode digital input pins. The 34710's Mode pins select the output voltage. For example, if Mode2, Mode1, and Mode0 are set to 0, 0, 0 (respectively) then $V_{I/O}$ will be set to 5.0V; if Mode2, Mode1, and Mode0 are all left floating (i.e., Open, Open, and Open), then the voltage for $V_{I/O}$ will be set to 3.3V. Table 5 provides the truth table for setting the various combination of regulator outputs via the Mode pins.

The topology of the regulator is a hysteretic buck regulator operating from the internal ~200kHz oscillator.

### $V_{CORE}$ Linear Regulator

The $V_{CORE}$ linear LDO (low drop-out) regulator can produce either a +3.3V, 2.5V, 1.8V, or 1.5V output voltage at currents up to 500mA. The input to the VCORE regulator is a pin that may be connected to the $V_{I/O}$ regulator output or to an external power supply. Note, the minimum input voltage level must be equal to or greater than the selected $V_{CORE}$ voltage + 0.8V. (I.e., 0.8V is the LDO regulator drop out voltage.)

The Mode pins select the output voltage as depicted in Table 5.

**Table 5. $V_{I/O}$ and $V_{CORE}$ Regulator Output Voltage Selection**

| Mode2 | Mode1 | Mode0 | $V_{I/O}$ (V) | $V_{CORE}$ (V) |
|---|---|---|---|---|
| 0 | 0 | 0 | 5.0 | 3.3 |
| 0 | 0 | Open | 3.3 | 2.5 |
| 0 | Open | 0 | 5.0 | 1.8 |
| 0 | Open | Open | 3.3 | 1.8 |
| Open | 0 | 0 | 5.0 | 2.5 |
| Open | 0 | Open | 3.3 | 2.5 |
| Open | Open | 0 | 5.0 | 1.5 |
| Open | Open | Open | 3.3 | 1.5 |

Open indicates pin is not connected externally (i.e. floating).

## *FUNCTIONAL PIN DESCRIPTION*

### POWER SUPPLY INPUT (B+)

Main supply voltage for the $V_{I/O}$ Switching Regulator and general chip bias circuitry.

### CORE VOLTAGE REGULATOR INPUT (LIN B+)

Supply voltage for the $V_{CORE}$ Regulator. May be provided by the $V_{I/O}$ regulator output or from an independent supply.

### MODE CONTROL (MODE 0,1,2)

Mode select pins to select the $V_{I/O}$ and $V_{CORE}$ output voltages per table 2. Pull to ground for low state, float for high state.

### SWITCHING CAPACITORS 1 AND 2 (CP1/CP2)

Pins for the Charge Pump capacitor.

### BOOST VOLTAGE (VB)

The Boost Voltage is an output pin used for the charge pump boost voltage and is a connection point for the Charge Pump bulk capacitor.It provides a gate drive for the $V_{I/O}$ Switch FET.

### RESET ($\overline{RST}$)

Reset is an output pin for supervisory functions. This pin is in high state during normal operation and low state during fault conditions. This pin has no input function and requires an external pull-up resistor.

The $\overline{RST}$ pin is an open drain output driver to prevent oscillations during the transition. It is recommended to connect a 0.1uF capacitor between the CT pin and $\overline{RST}$ pin. Note: error conditions must be present for a minimum time, $t_{FILTER}$, before the 34710 responds to them. Once all error conditions have been cleared, $\overline{RST}$ is held low for an additional time of $t_{DELAY}$.

### RESET DELAY CAPACITOR (CT)

This pin is the external delay. It is used with a capacitor to ground to delay $\overline{RST}$ turn-on time and to $\overline{RST}$ to prevent $\overline{RST}$ oscillations during chip power-on.

### VI/O SWITCHING REGULATOR FEEDBACK (VFB)

This pin is the feedback input for the $V_{I/O}$ Switching Regulator and the output of the regulator application.

### VI/O SWITCHING REGULATOR OUTPUT (VSWITCH)

This pin is the Switching output for the $V_{I/O}$ Buck Regulator. It has internal high side FET.

## SUPERVISORY FUNCTIONS

### Supervisory Circuitry

The supervisory circuitry provides control of the $\overline{\text{RST}}$ line, an open drain signal, based on system operating conditions monitored by the 34710. $V_{I/O}$, $V_{CORE}$, $V_{B+}$, and thermal shutdown (TSD) detectors in various parts of the chip are monitored for error conditions. $V_{I/O}$, $V_{CORE}$, $V_{B+}$, and thermal shutdown have both positive and negative-going thresholds for triggering the reset function.

The supervisor circuitry also ensures that the regulator outputs follow a predetermined power-up and power-down sequence. Specifically, the sequencing ensures that $V_{I/O}$ is never less than 0.9V below $V_{CORE}$. This means that $V_{CORE}$ - $V_{I/O}$ will be clamped at 0.5V, and that the $V_{CORE}$ regulator operation will be suppressed during startup and shutdown to ensure that $V_{CORE}$ - $V_{I/O}$ = 0.9V.

### VB Charge Pump

The high side MOSFET in the switching regulator (buck converter) requires a gate drive supply voltage that is biased higher than the B+ voltage, and this boosted voltage is provided by the internal charge pump and stored in a capacitor between the VB pin and the B+ pin. The charge pump operates directly from the B+ supply, and uses an internal oscillator operating at 200kHz.

### Internal Oscillator

The internal oscillator provides a 200kHz square wave signal for charge pump operation and for the buck converter.

# TYPICAL APPLICATIONS

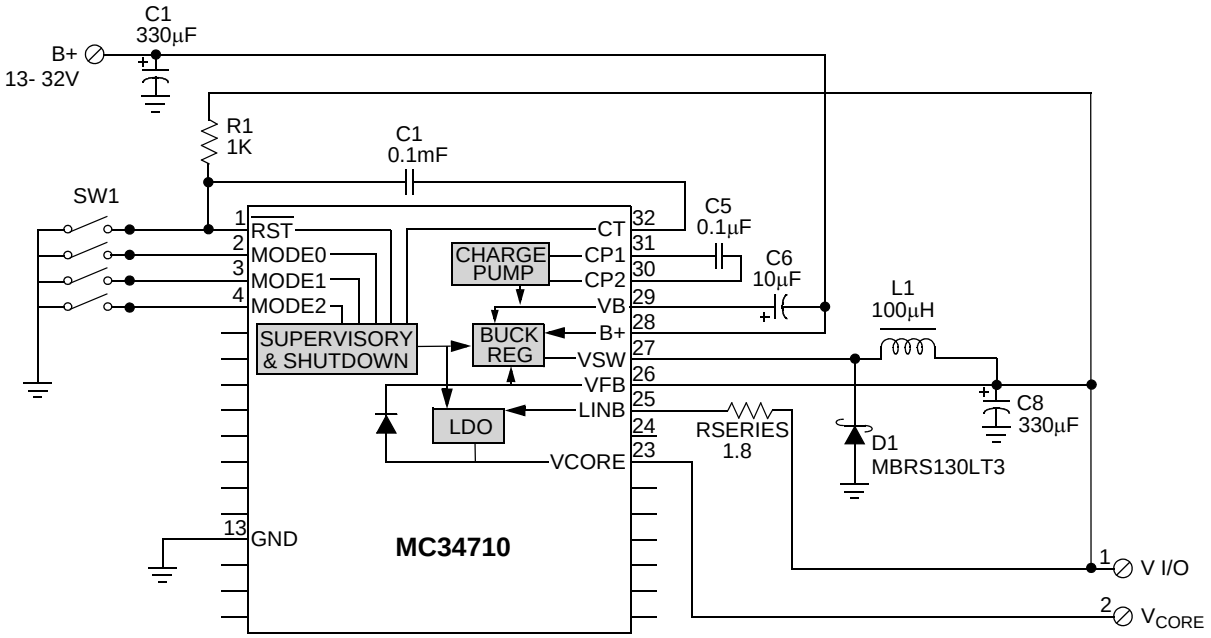



**Figure 4. Typical Application Diagram**

The MC34710 provides both a buck converter and an LDO regulator in one IC. Figure 4 above shows a typical application schematic for the MC34710. L1 is the buck converter's inductor. The buck inductor is a key component and must not only present the required reactance, but do so at a DC resistance of less than 20 milliohms in order to preserve the converter's efficiency. Also important to the converter's efficiency is the utilization of a low $V_F$ Schottky diode for D1.

Note that a 0.1uF capacitor is connected between CT and the reset pins; this prevents any possibility of oscillations occurring on the reset line during transitions by allowing the CT pin to discharge to ground potential via the $\overline{RST}$ pin, and then charge when $\overline{RST}$ returns to a logic high. The capacitor between the CP1 and CP2 pins is the charge pump's “bucket capacitor”, and sequentially charges and discharges to pump up the reservoir capacitor connected to the VB pin. Note that the reservoir capacitor's cathode is connected to B+ rather than ground. Also note that the charge pump is intended only to provide gate-drive potential for the buck regulator's internal power MOSFET, and therefore connecting external loads to the VB pin is not recommended.

The IC's internal $V_{CORE}$ LDO regulator can provide up to 500mA of current as long as the operating junction temperature is maintained below 105 degrees C. The heat-generating power dissipation of the LDO is primarily a function of the Volt x Amp product across the LINB+ and VCORE pins. Therefore, if the LINB+ voltage is >> than the selected $V_{CORE}$ voltage + 0.8V, it is recommended to use a power resistor in series with the LINB+ input to drop the voltage and dissipate the heat externally from the IC. For example, if the output of the buck regulator (V I/O on the schematic) is used as the input to LINB+, and the mode switches are set such that V I/O = 5V and $V_{CORE}$ = 3.3 , then a series resistance of 1.8 ohms at the LINB+ pin would provide an external voltage drop at 500mA while still leaving the minimum required headroom of 0.8V. Conversely, if the mode switches are set such that V I/O = 3.3V and $V_{CORE}$ = 2.5V, then no series resistance would be required, even at the maximum output current of 500mA.

Designing a power supply circuit with the MC34710, like all DC-DC converter ICs, requires special attention not only to component selection, but also to component placement (i.e., printed circuit board layout). The MC34710 has a nominal switching frequency of 200kHz, and therefore pcb traces between the buck converter discrete component pins and the IC should be kept as short and wide as possible to keep the parasitic inductance low. Likewise, keeping these pcb traces

short and wide helps prevent the converter's high di/dt switching transients from causing EMI/RFI.

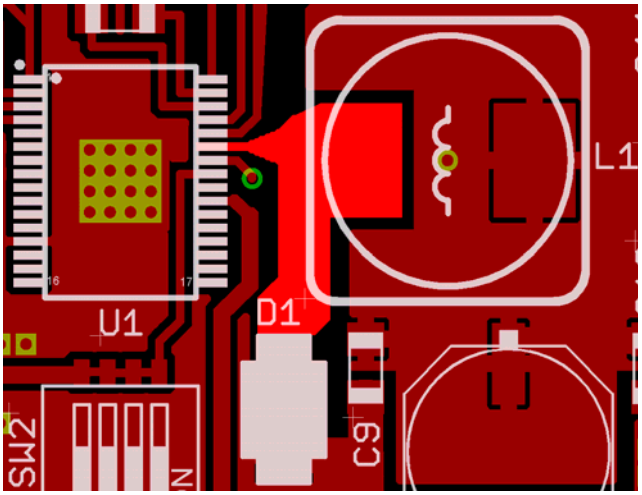



**Figure 5. Typical PCB Layout**

Figure 5 shows a typical layout for the pcb traces connecting the IC's switching pin (VSWITCH) and the power inductor, rectifier, and filter components.

Also, it is recommended to design the component layout so that the switching currents can be immediately sunk into a broad full-plane ground that provides terminations physically right at the corresponding component leads. This helps prevent switching noise from propagating into other sections of the circuitry.

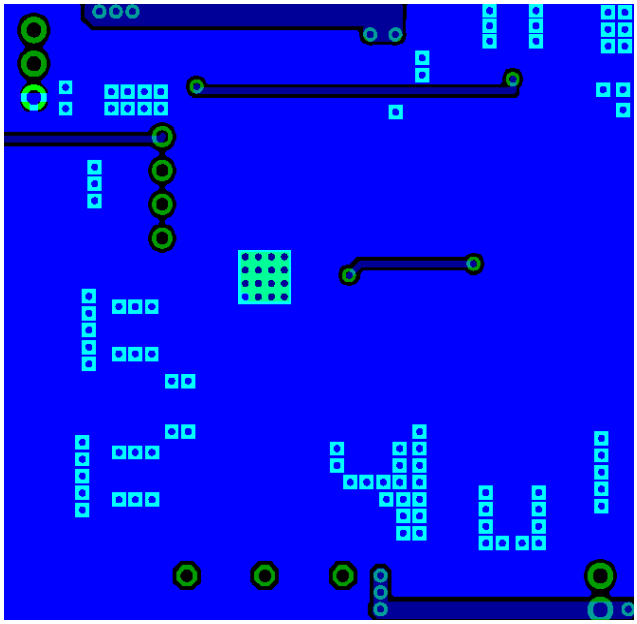


**Figure 6. Bottom Copper Layout**

Figure 6 illustrates a pcb typical bottom copper layout for the area underneath a buck converter populated on the top of the same section of pcb.

The ground plane is highlighted so the reader may note how the ground plane has been kept as broad and wide as possible. The square vias in the plane are located to provide an immediate path to ground from the top copper circuitry.

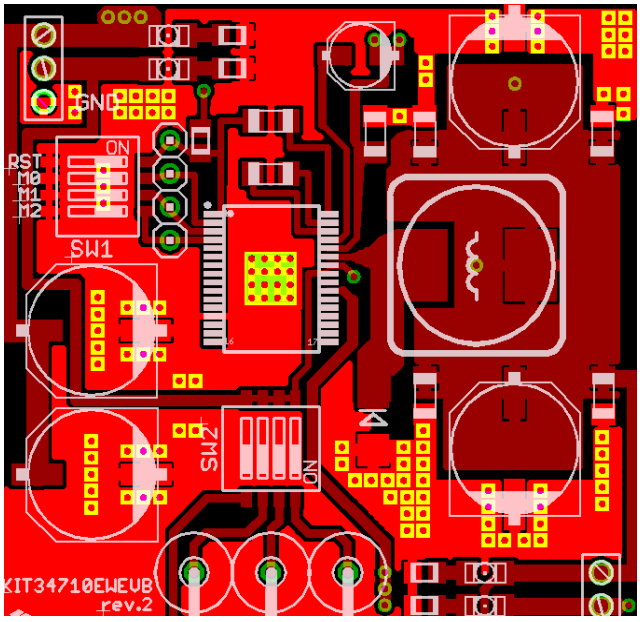



**Figure 7. Top Copper Layout**

Figure 7 shows the corresponding top copper circuit area with the component placement.

Again, the ground plane and the vias have been highlighted so the reader may note the proximity of these current sink pathways to the key converter components. It is also important to keep the power planes of the switching converter's output spread as broad as possible beneath the passive components, as this helps reduce EMI/RFI and the potential for coupling noise transients into adjacent circuitry.

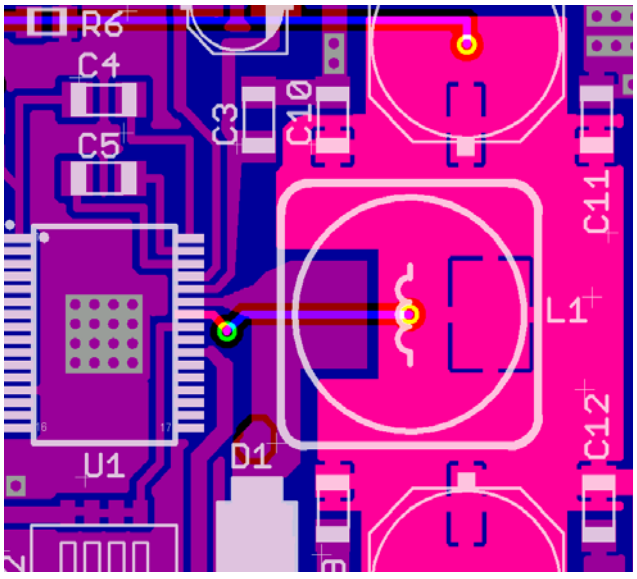



**Figure 8. Output Plane of Buck Converter**

Figure 8 shows the output plane of the buck converter highlighted.

This layout provides the lowest possible impedance as well as lowest possible dc resistance for the power routing. Note that the power path and its return should be placed, if possible, on top of each other on different layers or opposite sides of the pcb.

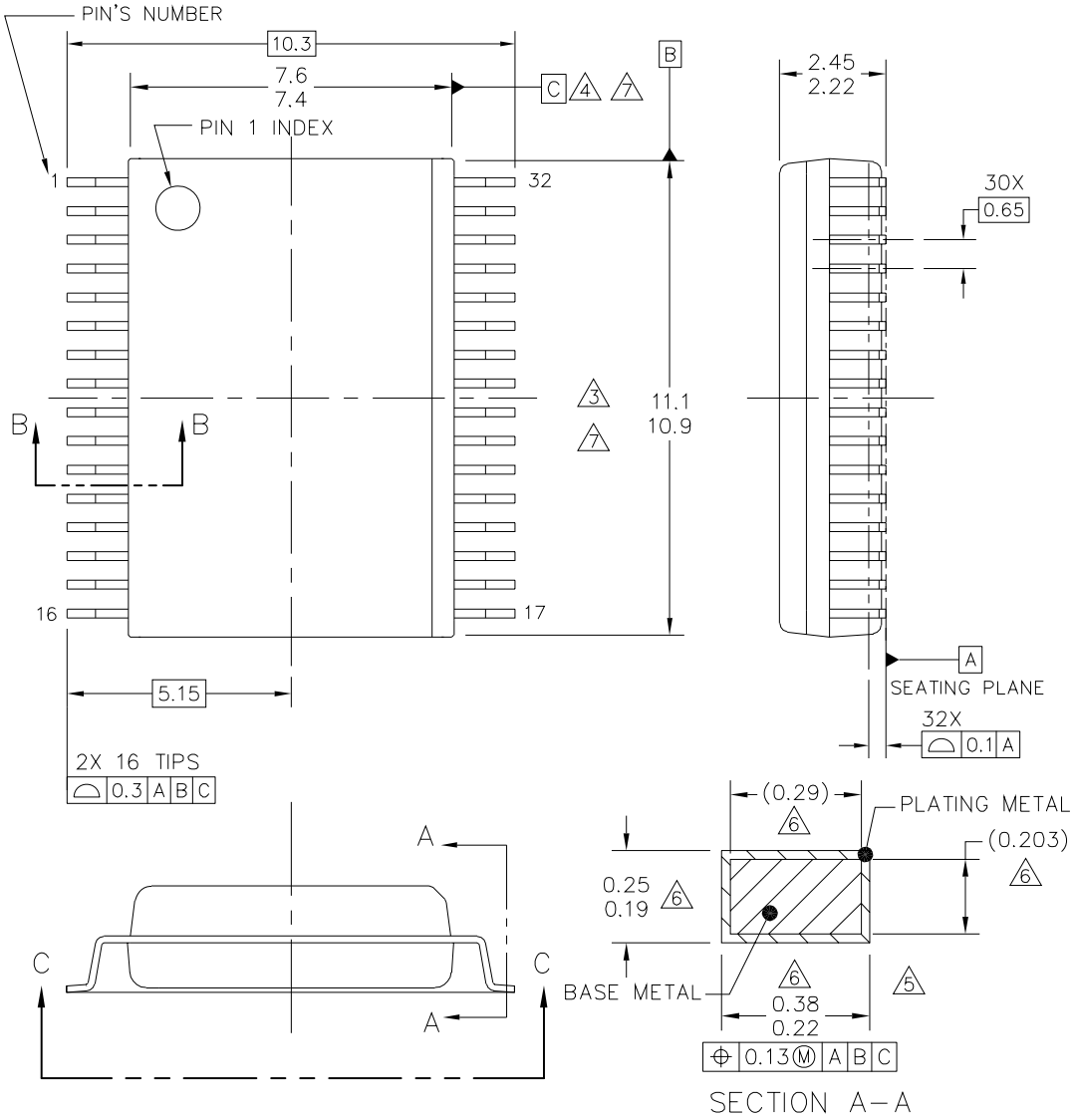
Small ceramic capacitors are placed in parallel with the Aluminum electrolytics so that the overall bulk filtering presents a low ESL to the high di/dt switching currents. Alternatively, special low ESL/ESR switching-grade electrolytics may be used.

An additional feature of the MC34710 is the 32 SOICW-EP exposed pad package. The package allows heat to be conducted from the die down through the exposed metal pad underneath the package and into the copper of the pcb. In order to best take advantage of this feature, a grid array of thru-hole vias should be placed in the area corresponding to the exposed pad, and these vias then should then connect to a large ground plane of copper to dissipate the heat into the ambient environment. An example of these vias can be seen in the previous figures of a typical pcb layout.

# PACKAGING

## *PACKAGE DIMENSIONS*

For the most current package revision, visit www.freescale.com and perform a keyword search using the “98A” listed below.

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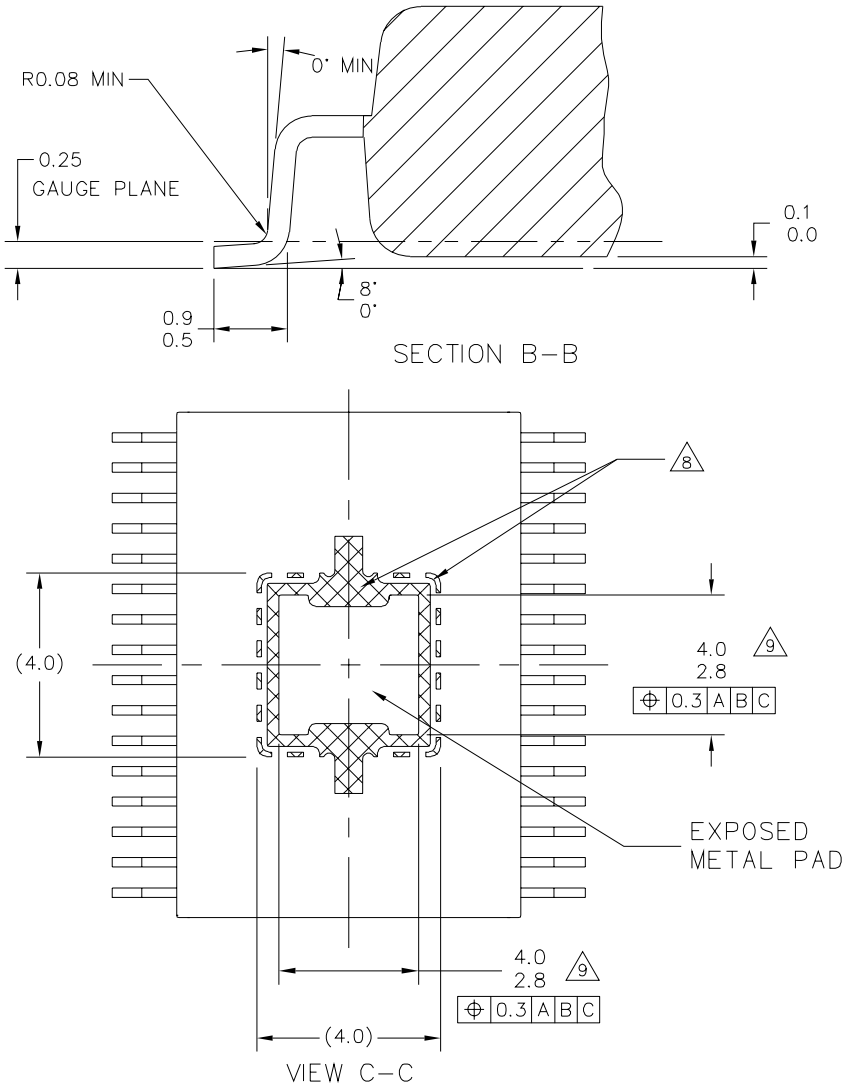
|---|---|---|
| TITLE: 32LD SOIC W/B, 0.65 PITCH 3.0 X 3.0 EXPOSED PAD, WITH MOLD LOCK CASE–OUTLINE | DOCUMENT NO: 98ASA10627D | REV: B |
| | CASE NUMBER: 1594–03 | 20 JUN 2008 |
| | STANDARD: NON–JEDEC | |

**EW (Pb-FREE) SUFFIX**
32-LEAD SOICW-EXPOSED PAD
98ASA10627D
ISSUE B

**34710**

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NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE.
4. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 mm.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.3 mm FROM THE LEAD TIP.
7. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER–LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
8. EXPOSED METAL AND MOLD FLASH MAY BE EXISTED IN THE HATCHED ZONE.
9. THESE DIMENSION RANGES DEFINE THE PRIMARY KEEP–OUT AREA. MOLD LOCKING AND RESIN BLEED CONTROL FEATURES MAY BE VISIBLE AND THEY MAY EXTEND TO 0.2mm FROM MAXIMUM EXPOSED PAD SIZE



| MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE |
|---|---|

| TITLE: | DOCUMENT NO: 98ASA10627D | REV: B |
|---|---|---|
| 32LD SOIC W/B, 0.65 PITCH<br>3.0 X 3.0 EXPOSED PAD, WITH MOLD LOCK<br>CASE–OUTLINE | CASE NUMBER: 1594–03 | 20 JUN 2008 |
| | STANDARD: NON–JEDEC | |

**EW (Pb-FREE) SUFFIX**
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**34710**

# REVISION HISTORY

| REVISION | DATE | DESCRIPTION OF CHANGES |
|---|---|---|
| 2.0 | 8/2008 | • Converted to Freescale format<br>• Updated Maximum Ratings, Static and Dynamic Characteristics tables.<br>• Updated packaging drawing<br>• Changed pin VI/O_OUT to VFB<br>• Implemented Revision History page |
| 3.0 | 3/2006 | • Updated format from Preliminary to Advance Information.<br>• Format and style corrections to match standard template. |
| 4.0 | 8/2008 | • Update the Freescale format and style<br>• Changed the reflow parameter name to Peak Package Reflow Temperature During Reflow(1), (2)<br>• Removed PC33710EW/R2 from the ordering information.<br>• Changed Advance status to Final<br>• Update the package drawing to Rev B. |

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